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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/635,902	08/11/00	HARADA	K 50090-234

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EXAMINER	
CHU,C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/22/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/635,902	HARADA ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 and 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figure 21 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

Specification

3. The disclosure is objected to because of the following informalities: on page 14, line 10, "semiconductor chip 1" should be --semiconductor chip 7--, because semiconductor chip 7 is a chip with insulation layer 6 on the backside of the chip, but the semiconductor chip 1 is not.

. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Nakazato et al.

Note Fig. 1 ~ Fig. 7 of Nakazato et al., where the reference shows a semiconductor device comprising: a semiconductor chip (10); at least a first electrode (11 in Fig. 3) formed on the first major surface of said semiconductor chip, at least a second electrode or an insulation layer (12 in Fig. 3 and 13 in Fig. 4) formed on the second major surface opposite to said first major surface (see Fig. 3 and Fig. 4); and at least a conductive member (20) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 3).

6. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Seidler.

Note Fig. 9 of Seidler, where the reference shows a semiconductor device comprising: a semiconductor chip (260 and 260'); at least a first electrode (262 and 262') formed on the first major surface of said semiconductor chip, at least a second electrode (264 and 264') or an insulation layer formed on the second major surface opposite to said first major surface (see Fig. 9); and at least a conductive member (210 and 210') for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 9).

Regarding claim 5, note Fig. 9 of Seidler, where the reference shows a semiconductor device comprising: a plurality of semiconductor device units (see Fig. 9), each of said semiconductor device units including: a semiconductor chip (260 and 260'); at least a first electrode (262 and 262') formed on the first major surface of said semiconductor chip (see Fig.

9), at least a second electrode (264 and 264') or an insulation layer formed on the second major surface opposite to said first major surface (see Fig. 9); and at least a conductive member (210 and 210') for connecting said first electrode with said second electrode or said insulation layer (see Fig. 9), said conductive member (210 and 210') being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 9); wherein said semiconductor device units are stacked each other, and said conductive members are connected to each other (see Fig. 9).

7. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Hatano et al.

Note Fig. 7 of Hatano et al., where the reference shows a semiconductor device comprising: a semiconductor chip (1); at least a first electrode (2) formed on the first major surface of said semiconductor chip, at least a second electrode or an insulation layer (3c) formed on the second major surface opposite to said first major surface (see Fig. 7); and at least a conductive member (4) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 7).

Regarding claim 5, note Fig. 8 of Hatano et al., where the reference shows a semiconductor device comprising: a plurality of semiconductor device units (see Fig. 8), each of said semiconductor device units including: a semiconductor chip (1); at least a first electrode (2) formed on the first major surface of said semiconductor chip (see Fig. 8), at least a second electrode or an insulation layer (3c) formed on the second major surface opposite to said first major surface (see Fig. 8); and at least a conductive member (4) for connecting said first

electrode with said second electrode or said insulation layer (see Fig. 8), said conductive member (4) being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 8); wherein said semiconductor device units are stacked each other, and said conductive members are connected to each other (see Fig. 8).

8. Claims 1, 3, 5, 8, 10, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto et al.

Note Fig. 5 of Sakamoto et al., where the reference shows a semiconductor device comprising: a semiconductor chip (300); at least a first electrode (310) formed on the first major surface of said semiconductor chip, at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface (see Fig. 5); and at least a conductive member (306) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 5).

Regarding claims 3, 8, and 12, note Fig. 5 of Sakamoto et al., where the reference shows each of said conductive members (306) is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer.

Regarding claim 5, note Fig. 5 of Sakamoto et al., where the reference shows a semiconductor device comprising: a plurality of semiconductor device units (see Fig. 5), each of said semiconductor device units including: a semiconductor chip (300); at least a first electrode (310) formed on the first major surface of said semiconductor chip (see Fig. 5), at least a second electrode or an insulation layer formed on the second major surface opposite to said first major

surface (see Fig. 5); and at least a conductive member (306) for connecting said first electrode with said second electrode or said insulation layer (see Fig. 5), said conductive member (306) being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 5); wherein said semiconductor device units are stacked each other, and said conductive members are connected to each other (see Fig. 5).

Regarding claim 10, note Fig. 5 of Sakamoto et al., where the reference shows a semiconductor device comprising: a plurality of semiconductor device units (see Fig. 5), each of said semiconductor device units including: a semiconductor chip (300); at least a first electrode (310) formed on the first major surface of said semiconductor chip (see Fig. 5), at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface (see fig. 5); and at least a conductive member (306) for connecting said first electrode with said second electrode or said insulation layer (see Fig. 5), said conductive member (306) being formed along the outer circumference of at least a side of said semiconductor chip (see Fig. 5); a packaging board (320) for mounting said plurality of semiconductor device units (see Fig. 5); wherein said semiconductor device units are placed on said packing board so as to have a predetermined angle to said packaging board (see Fig. 5), and said conductive members (306) of said semiconductor device units are connected to said packaging board (see Fig. 5).

9. Claims 14 ~ 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram et al.

Note Fig. 4 of Akram et al., where the reference shows a semiconductor device comprising: a plurality of semiconductor chips (14) each having electrodes formed on the major surface thereof (see Fig. 4), and a plurality of spacer members (10A, 10B, and 10C) each having

conductive pattern on the surface thereof (see Fig. 4); wherein said semiconductor chips (14) and said spacer members (10A ~ 10C) are stacked (see Fig. 4) alternately such that said electrodes of said semiconductor chips are electrically connected to said conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other (see Fig. 4).

Regarding claim 15, note Fig. 4 of Akram et al., where the reference shows each of said spacer members has a cavity for accommodating the end portion of said semiconductor chip (see Fig. 4).

Regarding claim 16, note Fig. 4 of Akram et al., where the reference shows further comprising supporting members having conductive pattern thereon, wherein said supporting members are placed so as to make said conductive patterns thereof contact with said conductive patterns of said plurality of spacer members (see Fig. 4).

10. Claims 14 ~ 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugano et al.

Note Fig. 46 of Sugano et al., where the reference shows a semiconductor device comprising: a plurality of semiconductor chips (302 in Fig. 47) each having electrodes (304 in Fig. 47) formed on the major surface thereof (see Fig. 46), and a plurality of spacer members (310 and 314 in Fig. 47) each having conductive pattern on the surface thereof (see Fig. 46); wherein said semiconductor chips (302 in Fig. 47) and said spacer members (310 and 314 in Fig. 47) are stacked (see Fig. 46) alternately such that said electrodes (304 in Fig. 47) of said semiconductor chips (302 in Fig. 47) are electrically connected (304 in Fig. 47) to said

conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other (see Fig. 46).

Regarding claim 15, note Fig. 46 of Sugano et al., where the reference shows each of said spacer members (310 and 314 in Fig. 47) has a cavity for accommodating the end portion of said semiconductor chip (see Fig. 46).

Regarding claim 16, note Fig. 46 of Sugano et al., where the reference shows further comprising supporting members having conductive pattern thereon (see Fig. 47), wherein said supporting members are placed so as to make said conductive patterns thereof contact with said conductive patterns of said plurality of spacer members (see Fig. 46).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 6, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. in view of Gaynes et al.

Sakamoto et al. discloses the claimed invention except each of said conductive members is comprised of a wire bonded to said first electrode and said second electrode. However, Gaynes et al. shows that a wire (172 in Fig. 17) to bond the first electrode and second electrode. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was

made to modify Sakamoto et al. by using a wire as taught by Gaynes et al. The ordinary artisan would have been motivated to modify Sakamoto et al. in the manner described above for at least the purpose of decreasing a cost of the manufacture.

Regarding claim 6, Sakamoto et al. discloses the claimed invention except a first chip has a first conducting pattern extended from said first electrode, a second chip has a second conducting pattern extended from said second electrodes, and a bump is provided between said first conducting pattern and said second conducting pattern, which face to each other, for electrically connecting said two conducting patterns. However, Gaynes et al. shows that a first chip has a first conducting pattern extended from said first electrode, a second chip has a second conducting pattern extended from said second electrodes, and a bump is provided between said first conducting pattern and said second conducting pattern, which face to each other, for electrically connecting said two conducting patterns (see Fig. 7 and Fig. 22). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Sakamoto et al. by adding a first conducting pattern on the first chip, a second conducting pattern on the second chip, and a bump between the first and second conducting pattern as taught by Gaynes et al. The ordinary artisan would have been motivated to modify Sakamoto et al. in the manner described above for at least the purpose of reducing connections exposure to electrical noise.

13. Claims 4, 9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. in view of Whitney et al.

Sakamoto et al. discloses the claimed invention except each of said conductive member is comprised of conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer. However, Whitney et al. shows that a conductive layer (70 and 80 in Fig. 1) to bond the first electrode and second electrode. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Sakamoto et al. by using a conductive layer as taught by Whitney et al. The ordinary artisan would have been motivated to modify Sakamoto et al. in the manner described above for at least the purpose of increasing reliability and operation of the package (column 1, lines 26 ~ 31).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kweon, Dennis, and Ono disclose stacked chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
August 17, 2001

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